

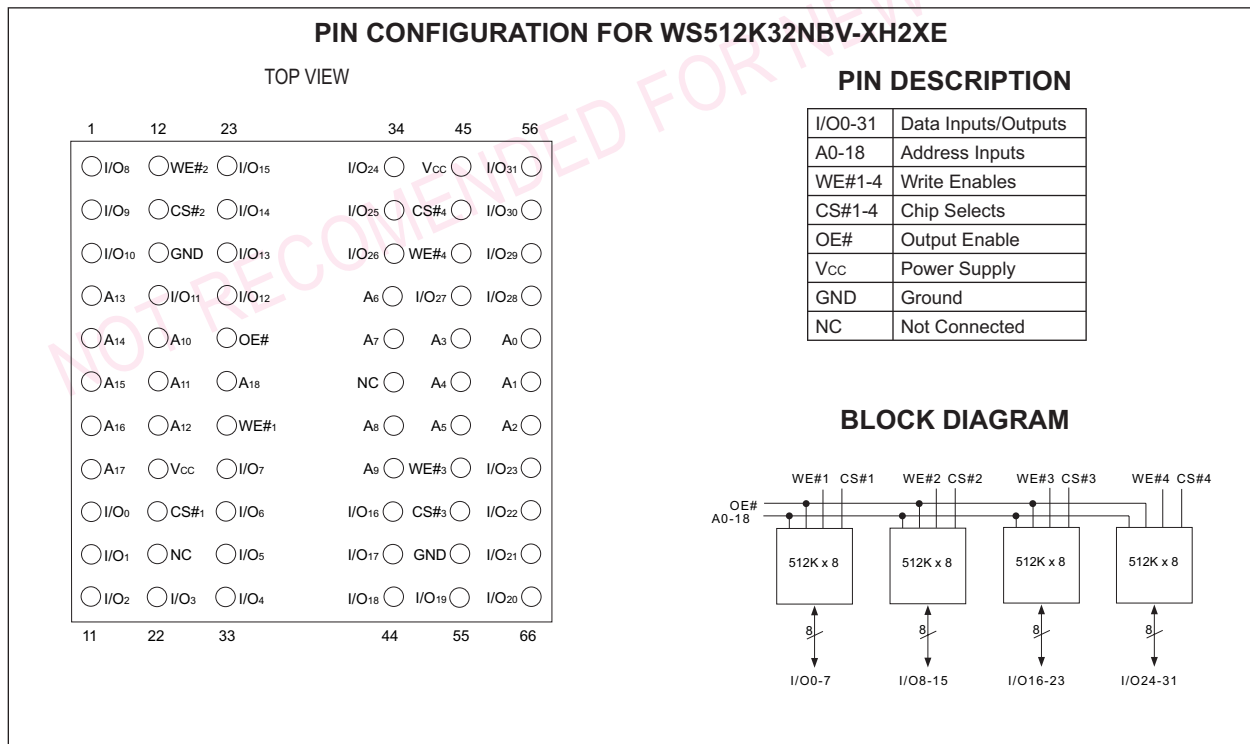


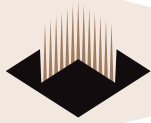
512Kx32 3.3V SRAM MODULE

FEATURES

- Access Times of 15*, 17, 20ns
- Low Voltage Operation
- Packaging
 - 66-pin, PGA Type, 1.385 inch square Hermetic Ceramic HIP (Package 402)
 - 68 lead, Hermetic CQFP (G2), 22mm (0.880 inch) square (Package 500). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint
- Organized as 512Kx32; User Configurable as 1Mx16 or 2Mx8
- Radiation Tolerant with Epitaxial Layer Die
- Commercial and Industrial Temperature Ranges
- 3.3V Power Supply
- BiCMOS
- TTL Compatible Inputs and Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
 - WS512K32BV-XG2XE - 8 grams typical
 - WS512K32NBV-XH2XE - 13 grams typical

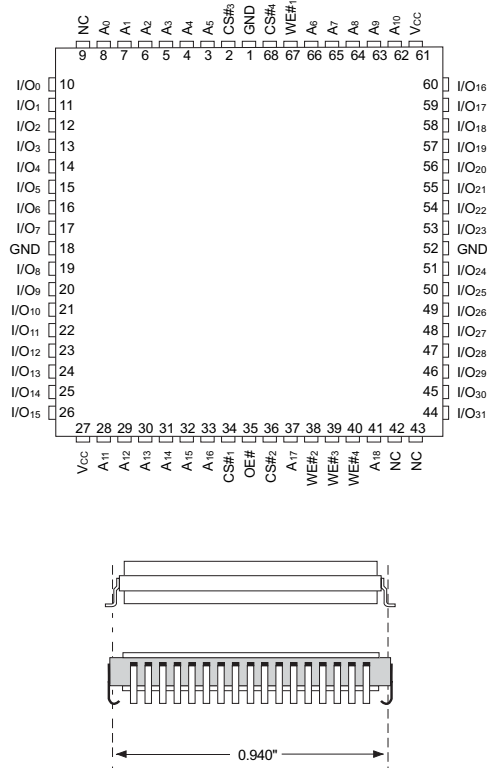
* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.





PIN CONFIGURATION FOR WS512K32BV-XG2XE

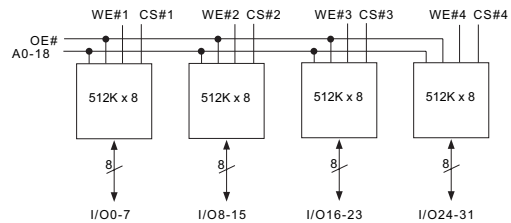
TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
WE#1-4	Write Enables
CS#1-4	Chip Selects
OE#	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



The WEDC 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-40	+85	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	4.6	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	4.6	V

TRUTH TABLE

CS#	OE#	WE#	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	3.0	3.6	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	50	pF
WE#1-4 capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
HIP (PGA)				
CQFP G2			20	
CS#1-4 capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 3.3V ± 0.3V, V_{SS} = 0V, T_A = -40°C to +85°C)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I _{LI}	V _{IN} = GND to V _{CC}		10	µA
Output Leakage Current	I _{LO}	CS# = V _{IH} , OE# = V _{IH} , V _{OUT} = GND to V _{CC}		10	µA
Operating Supply Current (x 32 Mode)	I _{CC} x 32	CS# = V _{IL} , OE# = V _{IH} , f = 5MHz, V _{CC} = 3.6V		480	mA
Standby Current	I _{SB}	CS# = V _{IH} , OE# = V _{IH} , f = 5MHz, V _{CC} = 3.6V		110	mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V



AC CHARACTERISTICS

(V_{CC} = 3.3V, T_A = -40°C to +85°C)

Parameter	Symbol	-15*		-17		-20		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle								
Read Cycle Time	t _{RC}	15		17		20		ns
Address Access Time	t _{AA}		15		17		20	ns
Output Hold from Address Change	t _{OH}	0		0		0		ns
Chip Select Access Time	t _{ACS}		15		17		20	ns
Output Enable to Output Valid	t _{OE}		7		8		10	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	2		2		2		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	0		0		0		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		7		8		10	ns
Output Disable to Output in High Z	t _{OHZ} ¹		7		8		10	ns

1. This parameter is guaranteed by design but not tested.

*Advanced information.

AC CHARACTERISTICS

(V_{CC} = 3.3V, T_A = -40°C to +85°C)

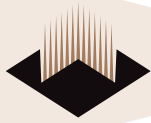
Parameter	Symbol	-15*		-17		-20		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle								
Write Cycle Time	t _{WC}	15		17		20		ns
Chip Select to End of Write	t _{CW}	10		12		14		ns
Address Valid to End of Write	t _{AW}	10		12		14		ns
Data Valid to End of Write	t _{DW}	8		9		10		ns
Write Pulse Width	t _{WP}	12		14		14		ns
Address Setup Time	t _{AS}	0		0		0		ns
Address Hold Time	t _{AH}	0		0		0		ns
Output Active from End of Write	t _{OW} ¹	2		3		3		ns
Write Enable to Output in High Z	t _{WHZ} ¹		8		8		9	ns
Data Hold Time	t _{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

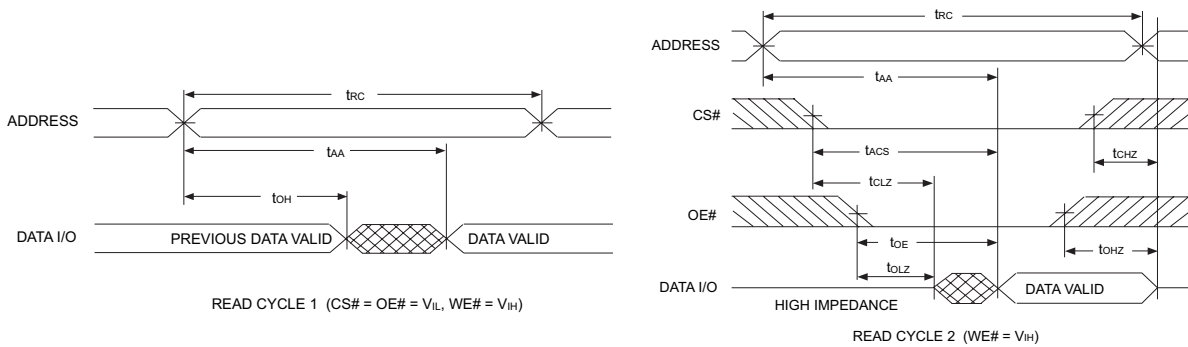
*Advanced information.

AC TEST CIRCUIT	AC TEST CONDITIONS															
	<table border="1" style="width: 100%;"> <thead> <tr> <th>Parameter</th> <th>Typ</th> <th>Unit</th> </tr> </thead> <tbody> <tr> <td>Input Pulse Levels</td> <td>V_{IL} = 0, V_{IH} = 2.5</td> <td>V</td> </tr> <tr> <td>Input Rise and Fall</td> <td>5</td> <td>ns</td> </tr> <tr> <td>Input and Output Reference Level</td> <td>1.5</td> <td>V</td> </tr> <tr> <td>Output Timing Reference Level</td> <td>1.5</td> <td>V</td> </tr> </tbody> </table> <p>NOTES: Vz is programmable from -2V to +7V. I_{OL} & I_{OH} programmable from 0 to 16mA. Tester Impedance Z₀ = 75 Ω. Vz is typically the midpoint of V_{OH} and V_{OL}. I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit. ATE tester includes jig capacitance.</p>	Parameter	Typ	Unit	Input Pulse Levels	V _{IL} = 0, V _{IH} = 2.5	V	Input Rise and Fall	5	ns	Input and Output Reference Level	1.5	V	Output Timing Reference Level	1.5	V
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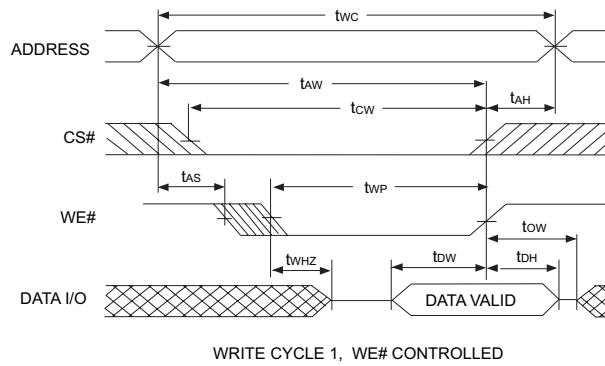
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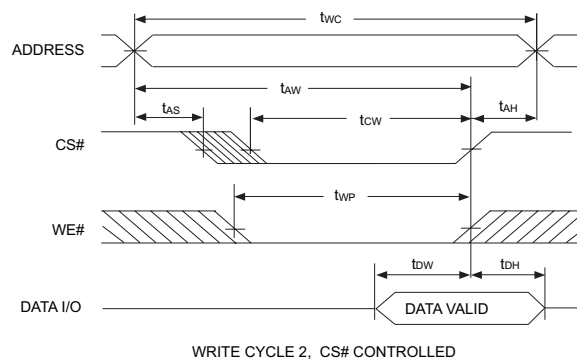
TIMING WAVEFORM - READ CYCLE

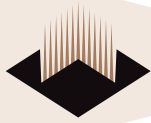


WRITE CYCLE - WE# CONTROLLED

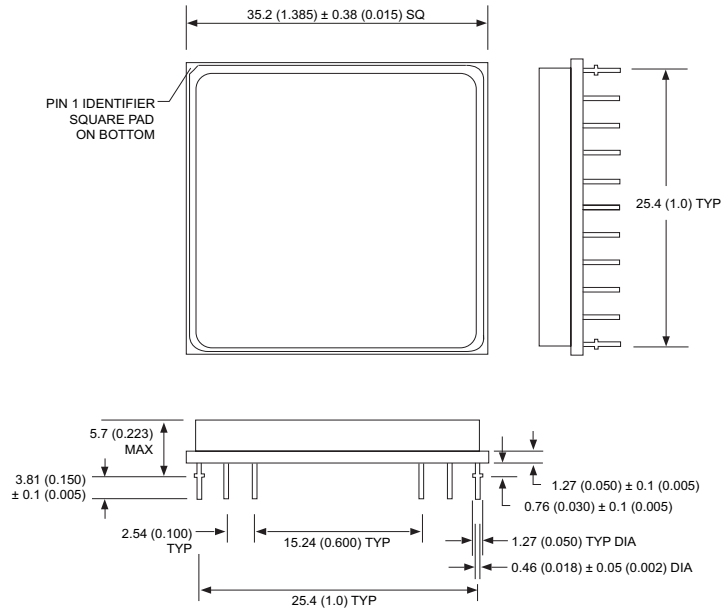


WRITE CYCLE - CS# CONTROLLED

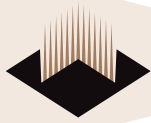




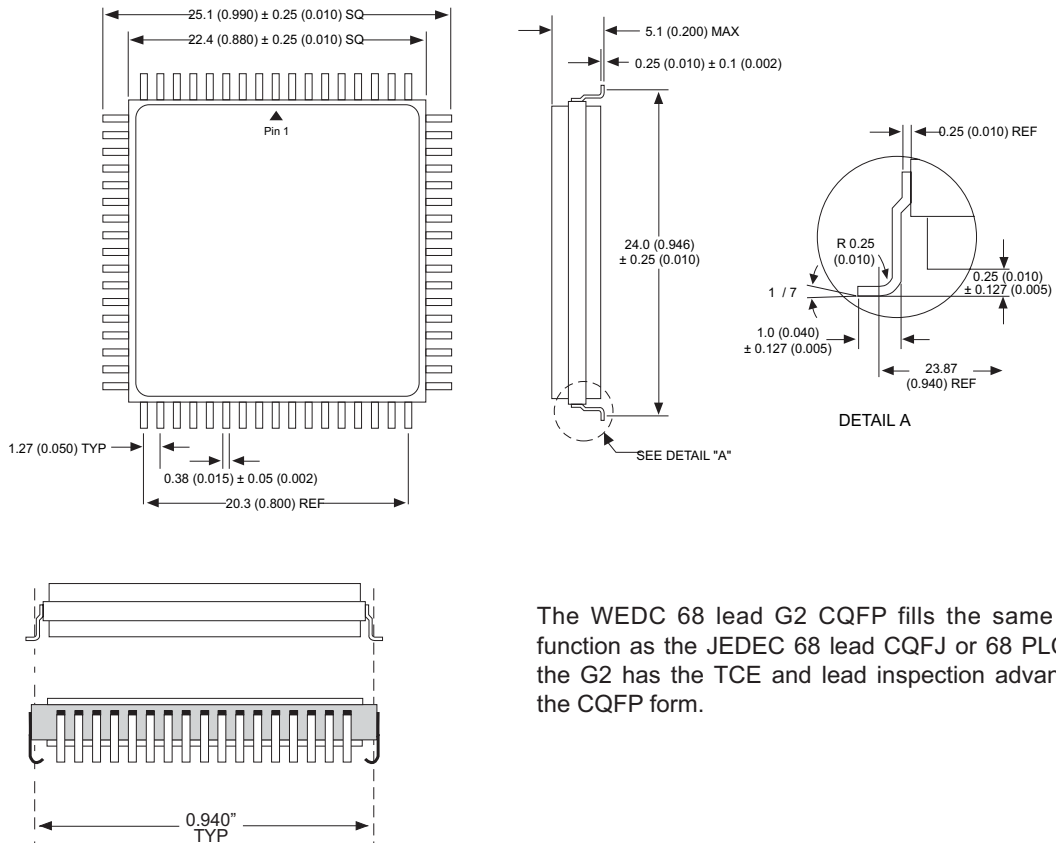
PACKAGE 402: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 500: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2)



The WEDC 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

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ORDERING INFORMATION

W S 512K 32 X B V - XXX X X E X

